# Design of Low Power 12-bit Magnitude Comparator

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*Abstract*—**The basic function in a microprocessor is magnitude comparison and also it is used in the field of digital signal processing, embedded systems so powerful magnitude comparator is needed. The objective of this paper is to provide small area, low power comparator for very large scale integration designers. in this paper a small power dissipation and less area over conventional 1 bit comparator is proposed and using this comparator a new style 12-bit comparator is proposed. Comparison between different designs is calculated by simulation that is performed at 0.25um technology in Tanner EDA Tool. It shows an 12-bit comparator of the proposed architecture only needs 196 transistors.**

*Keywords- Binary Comparator; Digital Arithmetic; High-Speed; Low Power; Magnitude Comparator.*

## I. INTRODUCTION

In digital system, comparison of two numbers is an arithmetic operation that determines if one number is greater than, equal to, or less than the other number [1]. So comparator is used for this purpose. Magnitude comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitudes (Fig.1). The outcome of comparison is specified by three binary variables that indicate whether A>B, A=B, or A<B[1-3].
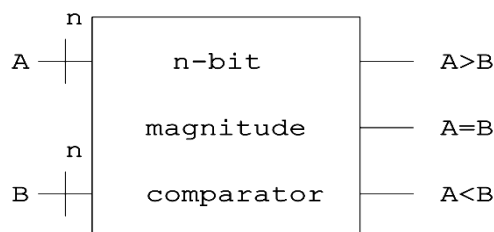


Figure 1. block diagram of n-bit magnitude comparator.

The circuit, for comparing two n-Bit numbers, has 2n inputs & 2 2n entries in the truth table, for 1-Bit numbers, 2-inputs & 4-rows in the truth table, similarly, for 2-Bit numbers 4-inputs & 16-rows in the truth table. The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. Circuit size depends on the number of transistors and their sizes and on the wiring complexity. The wiring complexity is determined by the number of connection s and their lengths. All these

characteristics may vary considerably from one logic style to another and thus proper choice of logic style is very important for circuit performance. In order to differentiate all designs, simulations are carried out for power, Delay, Power Delay Product at vdd=2.5v.Simulations are performed at 0.25um technology in Tanner EDA Tool v13.

## II. 1-BIT MAGNITUDE COMPARATOR

First of all we need to design an 1 bit comparator. We can easily make such a component, 2 bits for input A and B, and 2 bits for output X and Y. X is one when A is larger than B which means only when A is one and B is zero will set X to one. And for the Y, only when A and B both become one and zero will it be set. Here we can define.

$$X=AB' \qquad Y=AB+A'B'$$

TABLE I.    OPERATION TABLE FOR 1-BIT COMPARATOR.

| A | B | A>B | A=B |
|---|---|-----|-----|
| 0 | 0 | 0   | 1   |
| 0 | 1 | 0   | 0   |
| 1 | 0 | 1   | 0   |
| 1 | 1 | 0   | 1   |

Second we draw the Karnaugh-map of 1-bit comparator and find the relationship between the input and the output. And en (enable input) is for cascading purpose[26].

$$X=AB' \qquad \text{(When A>B)}$$

$$Y=AB+A'B' \text{ (When A=B)}$$

The circuit diagram of 1 bit comparator is shown in fig.2. Which is consist of Four two-input AND gates, One two-input NOR gate, Two inverters and one enable input.
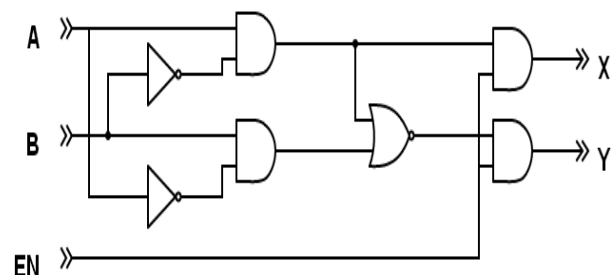


Figure 2.    Schematic of conventional 1-bit comparator

## A. TRANSISTOR IMPLEMENTATION

Fig. 3 shows the Transistor implementation of conventional 1-bit comparator. Actually the comparator implemented with CMOS logic for the above logic diagram. It is having the inputs A,B and EN inputs and X and Y as outputs. It takes 32 transistors to implement in CMOS technology.
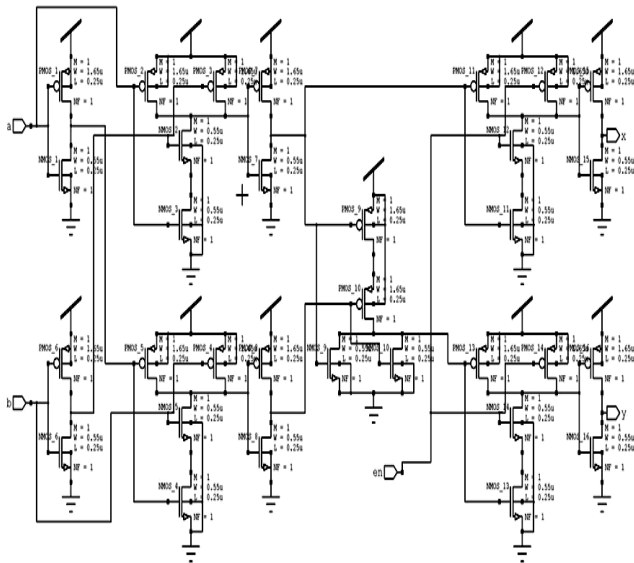


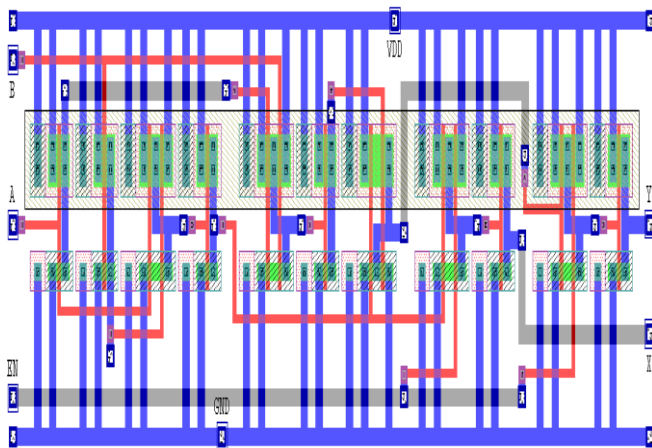Figure 3.    Transistor Implementation of conventional 1-bit comparator.

## B. LAYOUT



Figure 4.    Layout of conventional 1-bit comparator.

### III.    12-BIT MAGNITUDE COMPARATOR

The implementation of 12-bit comparator is shown in figure below. To neither implement this we need 12 1-bit comparators and one 12-input OR gate and a two input NOR gate. It has inputs (a11,b11 a10,b10 and so on up to a0,b0).and for each comparator we have x and y as out puts. Out put y is connected to enable input of each comparator and each x input is connected to 12-input OR gate. Last comparator y out and out put of 12-input OR gate is connected to the two input NOR gate. The below comparator consists of out puts P, Q and R. Each one has some indication means that P=1(when a>b),Q=1(when a<b) and R=1(when a=b).
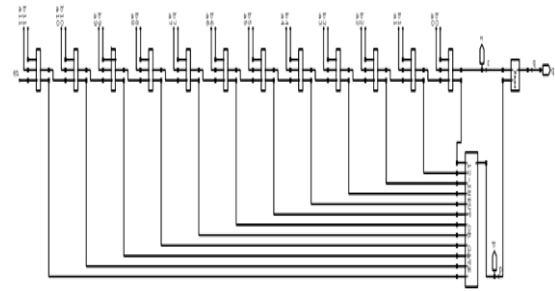


Figure 5.    Schematic of conventional 12-bit comparator.

From the above figure to construct 12-bit comparator it needs one 12-input OR Gate and one two input NOR gate. These two are for implementing p,q and r out puts. The gates used in this method is listed below:

## A. 12-bit  CMOS  OR gate:

It has 12 inputs namely in12,i11,etc to in0 and single output. It is implemented with CMOS technology. And also drawn layout using single metal1.generally OR gate can be implemented from NOR gate and an inverter connected at the output of the NOR gate. The parameters taken for both schematic and layout is wp=1.65um,wn=0.55um and vdd=2.5v for all simulations.
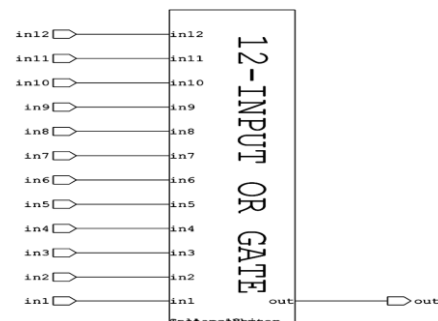


Figure 6.    Block diagram of 12 input OR gate

The functionality of 12 input OR gate can be implemented with CMOS logic. The biggest advantage of CMOS logic is it has full swing voltage levels and also it consumes less static power compared to the other technologies and also it takes more area compared to other  technologies. The layout of this CMOS OR gate implemented with double metals namely matal1 and metal2 and also via1 to bridge the connection between them.

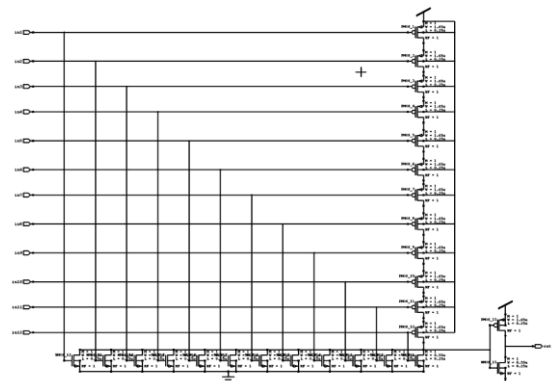## B. TRANSISTOR IMPLEMENTATION



Figure 7.    Transistor  Implementation  of  CMOS 12-input OR gate.

In the above figure 7 it contains both NMOS and PMOS. The principle of CMOS logic design says that Pull up network has only PMOS circuitry & Pull down network has only NMOS circuitry. The function of PUN is to provide connection between output & VDD, similarly of PDN is to provide connection between output & GND shown in figure 8.PUN and PDN networks are constructed in a fashion such that one & only one network is conducting at a time. Number of transistors for N-input logic gate is 2N. Any logic function can be realized by NMOS pull -down and PMOS pull-up networks connected between the gate output and the power lines. For CMOS technology it needs 2n number of transistors.
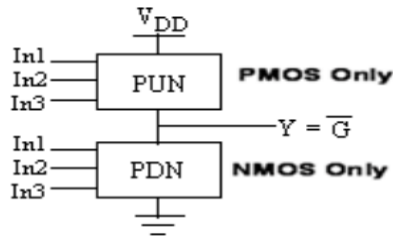


Figure 8. Logic Network of CMOS Style.

**Advantages**

- Design provides full output voltage swing between 0 and VDD.
- It provides high noise immunity because it has low sensitivity to noise.
- Provides high noise margin because VOH & VOL are nearly at VDD & GND, respectively.
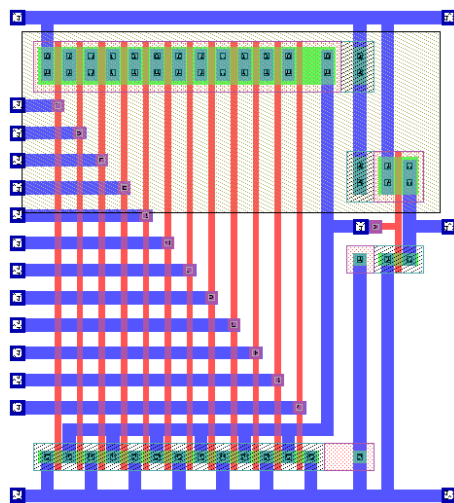- It is called Ratio less logic due to balanced device.

*C. LAYOUT:*



Figure 9. Layout of conventional 12-input OR gate.
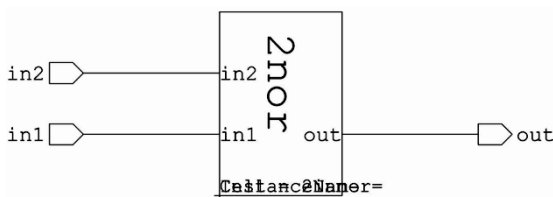
*D. 2-bit cmos NOR gate:*



Figure 10. Block diagram of 2 input NOR gate.
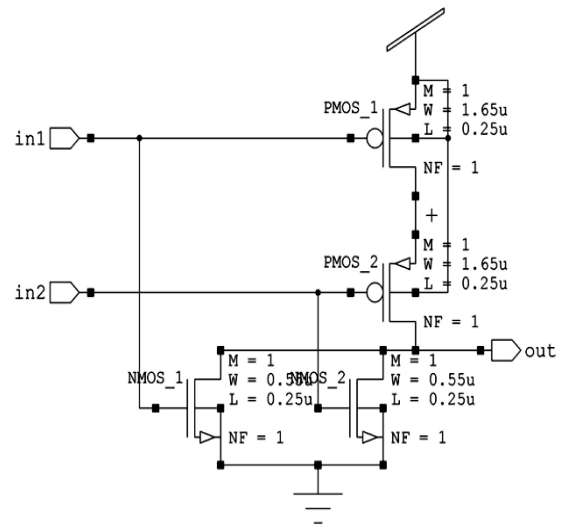
*E. TRANSISTOR IMPLEMENTATION*



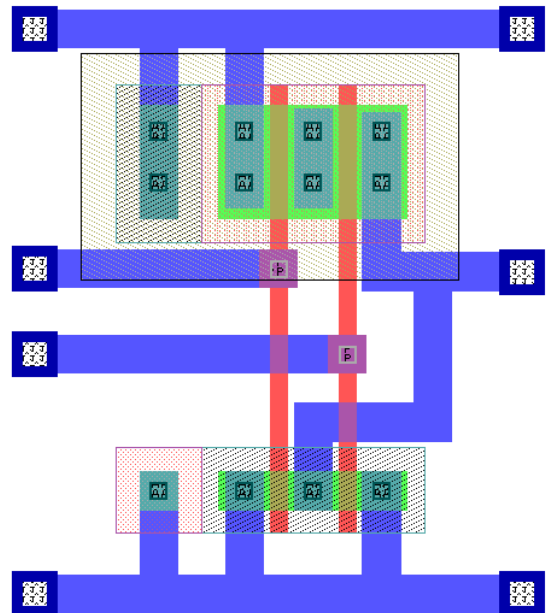Figure 11. Transistor Implementation of CMOS 2-input NOR gate.

*F. LAYOUT:*



Figure 12. Layout of 2-input NOR gate
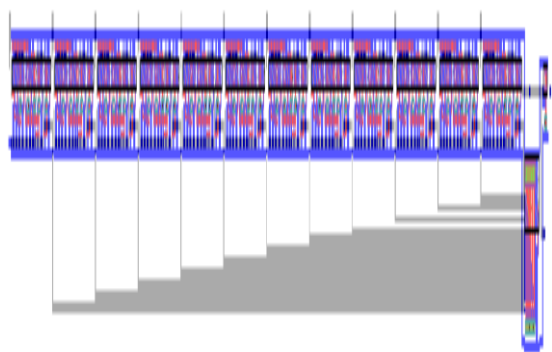
*G. 12-bit comparator layout:*



Figure 13. layout of conventional 12-bit comparator.
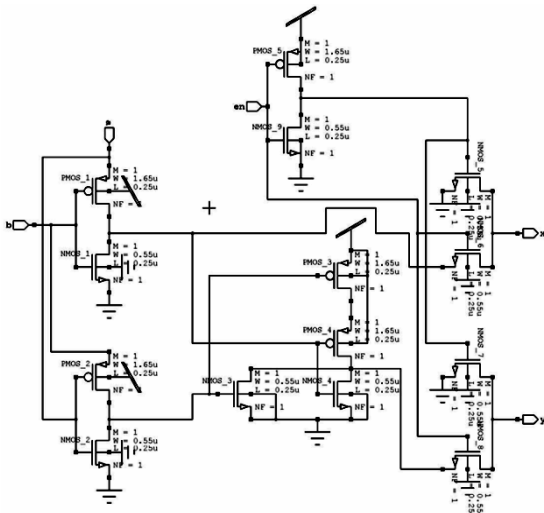
## IV. PROPOSED LOW POWER 1-BIT COMPARATOR:



Figure 14. Transistor Implementation of low power 1-bit comparator.

The above figure shows the proposed low power comparator. It is implemented with pass transistor logic and also in middle stage it is implemented with CMOS logic. It is very efficient in terms of power and area because the number of transistors required to implement proposed comparator is less when compared to the conventional comparator. And inputs to this comparator is a and b and outputs to this comparator is x and y. Enable input signal is used for cascading purpose.

The design parameters to implement this comparator is wp=1.65u and wn=0.55u.
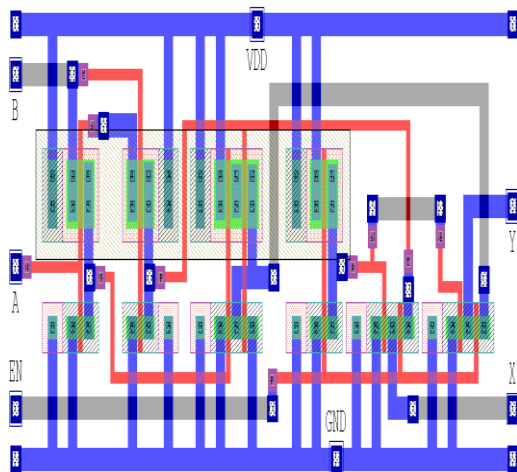
### A. LAYOUT:



Figure 15. layout of low power 1-bit comparator.

### B. Pass Transistor Logic (PTL):

Main idea behind PTL is to use purely NMOS Pass Transistors network for logic operation. The basic difference of pass-transistor logic style compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines as in Fig.13. In this design style, transistor acts as switch to pass logic levels from input to output. Schematic of AND Gate using Pass Transistor Logic in Fig.15 [15].
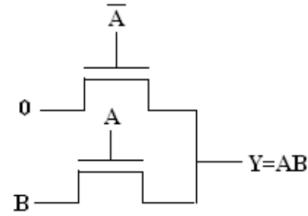


Figure 16. Symbol for AND Gate using Pass Transistor Logic.

Advantages:
- Design requires less number of transistors because one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation.
- Speed is increased because less number of transistors are used for design.
- Less area is required for design because PMOS is not used.

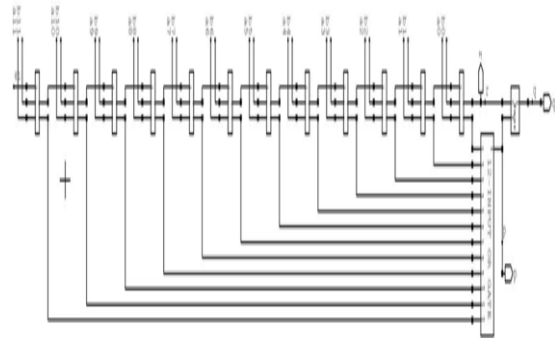## V. PROPOSED 12-BIT LOW POWER COMPARATOR:



Figure 17. Schematic of low power 12-bit comparator.

The implementation of 12-bit comparator is shown in figure.15 to implement this we need 12 1-bit low power comparators and one 12-input OR gate and a two input NOR gate. It has inputs (a11,b11 a10,b10 and so on up to a0,b0). And for each comparator we have x and y as out puts. Out put y is connected to enable input of each comparator and each x input is connected to 12-input OR gate. last comparator y out and out put of 12-input OR gate is connected to the two input NOR gate. The below comparator consists of out puts P,Q and R. Each one has some indication means that P=1(when a>b),Q=1(when a<b) and R=1(when a=b).

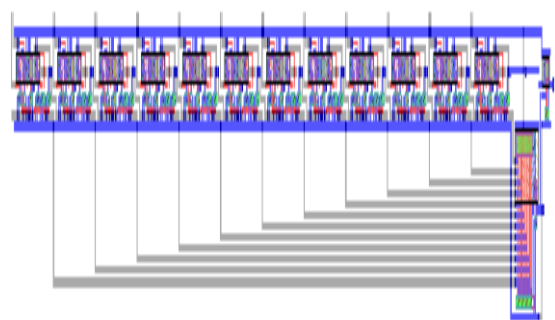### A. 12-bit low power comparator layout:



Figure 18. layout of conventional 12-bit low power comparator.

## VI. SIMULATION RESULTS:
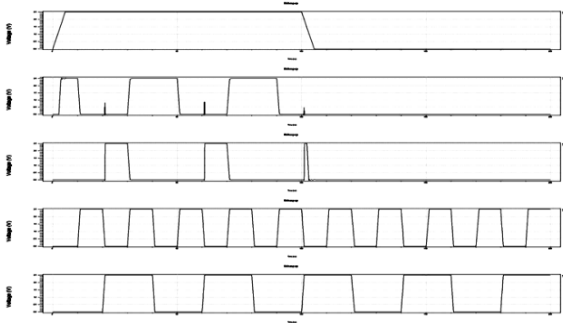
### A. Conventional 1 bit comparator:



Figure 19. Simulation for 1bit conventional comparator.
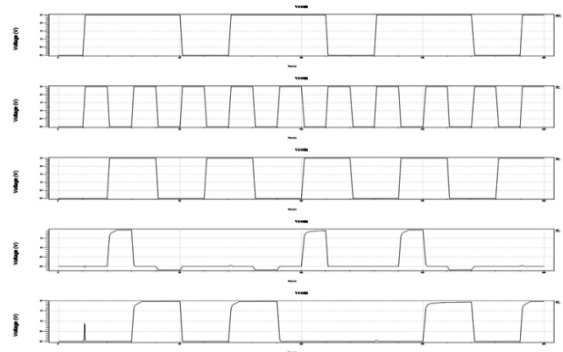
### B. low power 1 bit comparator:



Figure 20. Simulation for low power 1bit conventional comparator.

### C. 12 bit conventional comparator:
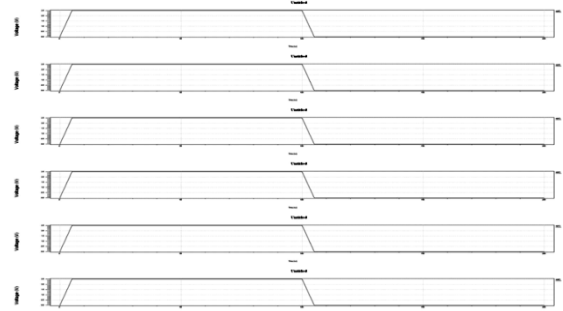
Inputs:

A0-a5:



Figure 21. Simulation for 12 bit conventional comparator.

A6-a11:
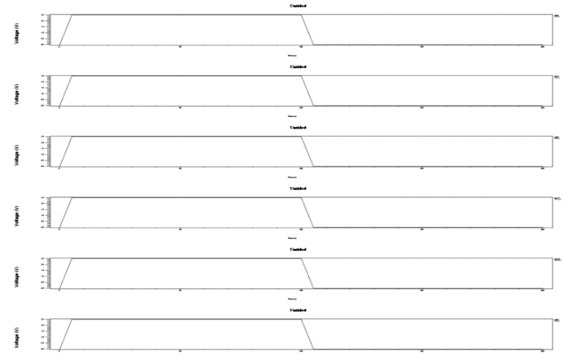


Figure 22. Simulation for 12 bit conventional comparator.

B0-b5:
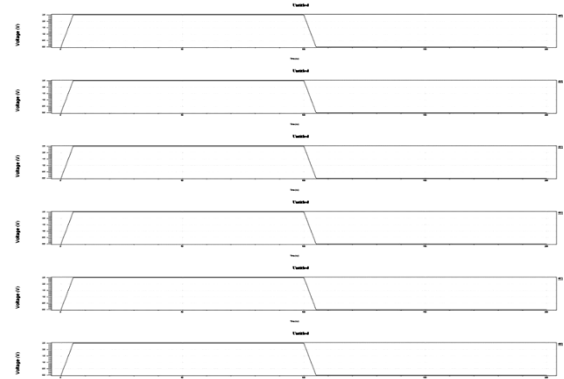


Figure 23. Simulation for 12 bit conventional comparator.

B6-b11:
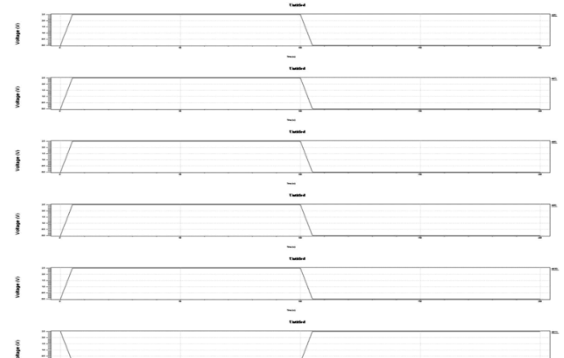


Figure 24. Simulation for 12 bit conventional comparator.

En,p,q,r:
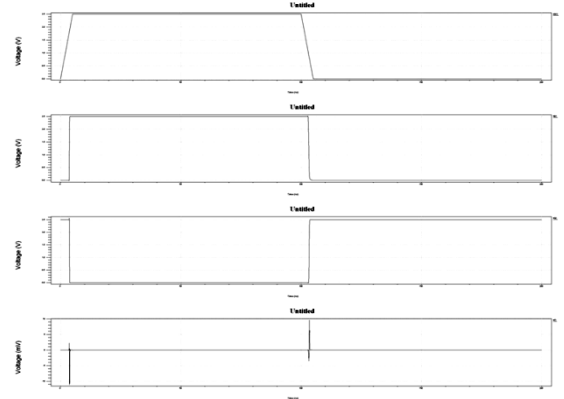


Figure 25. Simulation for 12 bit conventional comparator.

*Power Results:*

TABLE II.        POWER RESULTS

| Vdd=2.5v,cl=1fF | Power dissipation(w) | Delay(s) | PDP(w-s) |
|---|---|---|---|
| 1bit conv comparator | 3.45e-005 | 1.0267e-008 | 3.542e-013 |
| 12bit conv comparator | 1.6454e-004 | 1.0184e-009 | 1.6756e-013 |
| 1bit low power comparator | 4.191e-006 | 1.0068e-008 | 4.2194e-014 |
| 12 bit low power comparator | 1.743e-005 | 1.153e-009 | 2.0096e-014 |

*Area Results:*

TABLE III.        AREA RESULTS

| | Area(μm²) |
|---|---|
| 1bit conv comparator | 439.54 |
| 12bit conv comparator | 2445.93 |
| 1bit low power comparator | 200.713 |
| 12 bit low power comparator | 1655.69 |

## VII.    CONCLUSION AND FUTUREWORK

With power and area being a limiting factor in high density and high-performance VLSI designs, a great deal of effort has been made to explore low-power and area design options without sacrificing performance. After simulation of all four designs final results are obtained for Power Consumption, Delay, Power Delay Product. PTL Logic Style provides low power design as compared to  CMOS Logic Style. PTL Logic Style provides less PDP as compared to CMOS  logic style. It has been found that transistor count is less in PTL style  design than that of CMOS logic style  design.  An important factor, output voltage swing is better in CMOS logic style design & Transmission Gate design. But Transmission Gate logic style requires transistor count more than CMOS design style.PTL style do not provide full output voltage swing. Power, delay and PDP for low power comparator is less than the conventional comparator. In future the design of comparator will take less number of transistors than the existing one with low power and high PDP value. The comparisons of comparator design are based upon BSIM3V3 250nm technology in tanner EDA tool.

## ACKNOWLEDGMENT

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